

**What is claimed is:**

1           1.    An integrated circuit on a chip, comprising:  
2               a substrate; and  
3               at least one scan chain disposed in the substrate, with  
4               scan cells connected to form a series chain, each  
5               connection being formed according to a layout  
6               constraint with a minimum dimension provided by  
7               design rules for an assigned routing layer.

1           2.    The integrated circuit as claimed in claim 1,  
2               wherein the assigned routing layer is a first metal layer.

1           3.    The integrated circuit as claimed in claim 2,  
2               wherein the layout constraint limits the connection to passage  
3               through at least the first metal layer.

1           4.    The integrated circuit as claimed in claim 3,  
2               wherein the layout constraint limits the connection to passage  
3               through only the first metal layer.

1           5.    The integrated circuit as claimed in claim 3,  
2               wherein the layout constraint limits each metal line of the  
3               first metal layer, to form the connection, to line width of  
4               critical dimension (CD) of the first metal layer.

1           6.    The integrated circuit as claimed in claim 3,  
2               wherein the layout constraint further limits any metal line  
3               of a second metal layer in the connection to a line width  
4               exceeding CD of the second metal layer.

1           7.    The integrated circuit as claimed in claim 3,  
2    wherein the layout constraint further requires any plug of  
3    a plug layer linking two metal lines in the connection to be  
4    more than one.

1           8.    The integrated circuit as claimed in claim 1,  
2    wherein the assigned routing layer is a plug layer.

1           9.    The integrated circuit as claimed in claim 8,  
2    wherein the layout constraint limits the connection to passage  
3    through at least the plug layer and plugs of the plug layer,  
4    linking two metal lines in the connection, to one only.

1           10.   The integrated circuit as claimed in claim 9,  
2    wherein the layout constraint further limits any metal line  
3    of a metal layer in the connection to a line width exceeding  
4    CD of the metal layer.

1           11.   The integrated circuit as claimed in claim 1,  
2    wherein the integrated circuit further has an auxiliary  
3    routing net positioned in parallel beside the scan chain, the  
4    auxiliary routing net has metal lines of different lengths,  
5    and the auxiliary routing net does not function when the scan  
6    chain is originally formed.

1           12.   The integrated circuit as claimed in claim 11,  
2    wherein one of the metal lines has sufficient length to replace  
3    one of the connections in the scan chain.

1           13.   The integrated circuit as claimed in claim 11,  
2    wherein one of the metal lines has a length equal to at least  
3    two scan cells in the scan chain.